

TFT LCD Evaluation Specification

MODEL NO.: V420H1 – L11

- CONTENTS -

1. GENERAL DESCRIPTION	-----3
1.1 OVERVIEW	
1.2 FEATURES	
1.3 APPLICATION	
1.4 GENERAL SPECIFICATIONS	
1.5 MECHANICAL SPECIFICATIONS	
2. INPUT TERMINAL PIN ASSIGNMENT	-----4
2.1 TFT LCD MODULE INPUT	
2.2 INVERTER UNIT PIN ASSIGNMENT	
2.3 BLOCK DIAGRAM OF INTERFACE	
2.4 LVDS INTERFACE	
3. COLOR DATA INPUT ASSIGNMENT	-----13
3.1 TFT LCD MODULE	
3.2 BACKLIGHT UNIT	
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS	
3.2.2 INVERTER CHARACTERISTICS	
3.2.3 INVERTER INTERFACE CHARACTERISTICS	
4. INTERFACE TIMING	-----15
4.1 INPUT SIGNAL TIMING SPECIFICATIONS	
5. PRECAUTIONS	-----17
5.1 ASSEMBLY AND HANDLING PRECAUTIONS	
5.2 SAFETY PRECAUTIONS	

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H1-L11 is a 42" TFT Liquid Crystal Display module with 16-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (400 nits)
- High contrast ratio (2000:1)
- Fast response time (6.5 ms)
- High color saturation (NTSC 72%)
- HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option

1.3 APPLICATIONS

- TFT LCD TVs

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	938.3 (H) x 531.3 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti Glare	-	(2)

Note (2) The specification of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	982.0	983.0	984.0	mm	(1), (2)
	Vertical (V)	575.0	576.0	577.0	mm	
	Depth (D)	53.5	54.5	55.5	mm	
Weight		12200	12700	13200	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. INPUT TERMINAL PIN ASSIGNMENT

2.1 TFT LCD Module Input

FI-RE51S-HF (JAE) or equivalent

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(2)
8	RPF	Display Rotation	(3)
9	ODSEL	Overdrive Lookup Table Selection	(4)
10	DGMEN	Dynamic Gamma Enable	(5)
11	DCREN	Dynamic Contrast Ratio Enable	(6)
12	ORX0-	Second pixel Negative LVDS differential data input. Channel 0	
13	ORX0+	Second pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Second pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Second pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Second pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Second pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Second pixel Negative LVDS differential clock input.	
20	OCLK+	Second pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Second pixel Negative LVDS differential data input. Channel 3	
23	ORX3+	Second pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ERX0-	First pixel Negative LVDS differential data input. Channel 0	
29	ERX0+	First pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	First pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	First pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	First pixel Negative LVDS differential data input. Channel 2	

33	ERX2+	First pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	First pixel Negative LVDS differential clock input.	
36	ECLK+	First pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	First pixel Negative LVDS differential data input. Channel 3	
39	ERX3+	First pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	GND	Ground	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low : VESA LVDS Format (default), High : JEIDA Format.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) Low : function disable (default), High : Dynamic Gamma function enable.

Note (6) Low : function disable (default), High : Dynamic Contrast Ratio function enable.

Note (7) Low =Open or Connect to GND, High = Connect to +3.3V

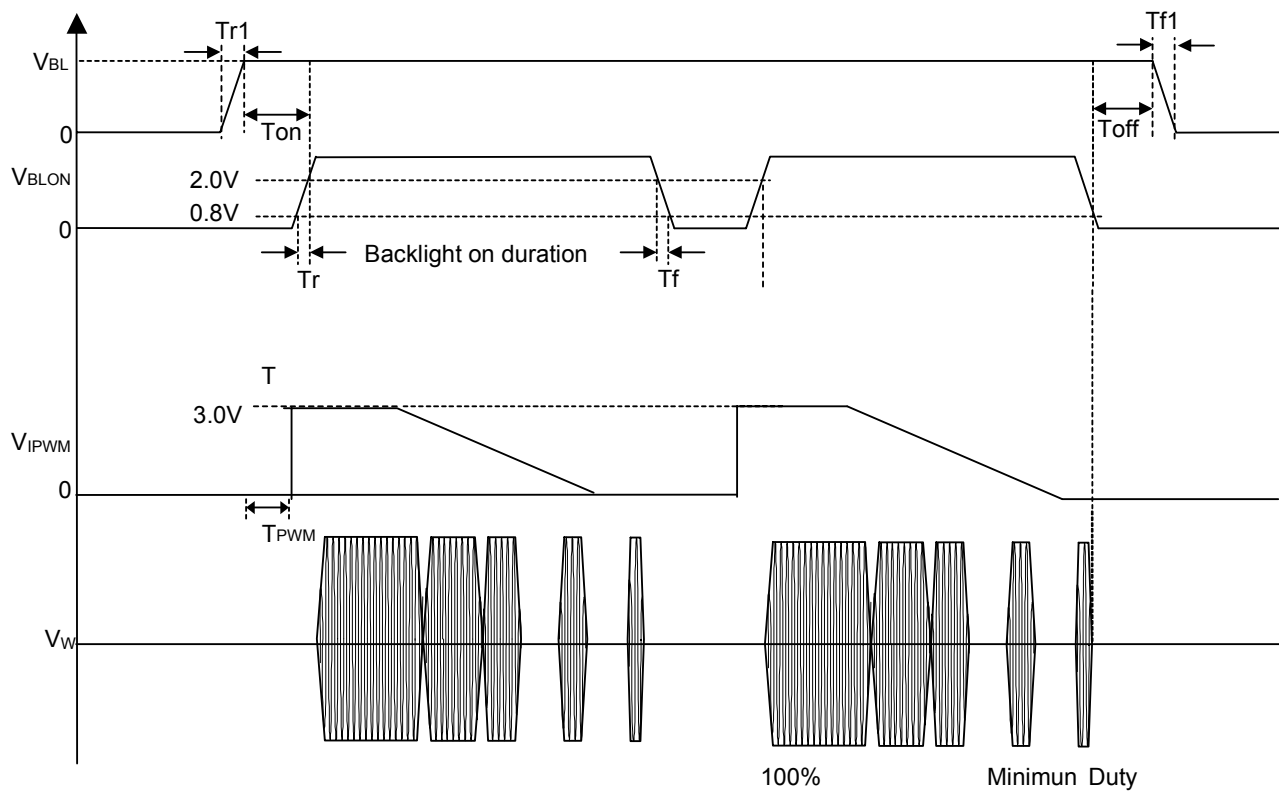
2.2 INVERTER UNIT PIN ASSIGNMENT

CN1: S12B-PH-SM3-TB(D)(LF)(JST) or equivalent

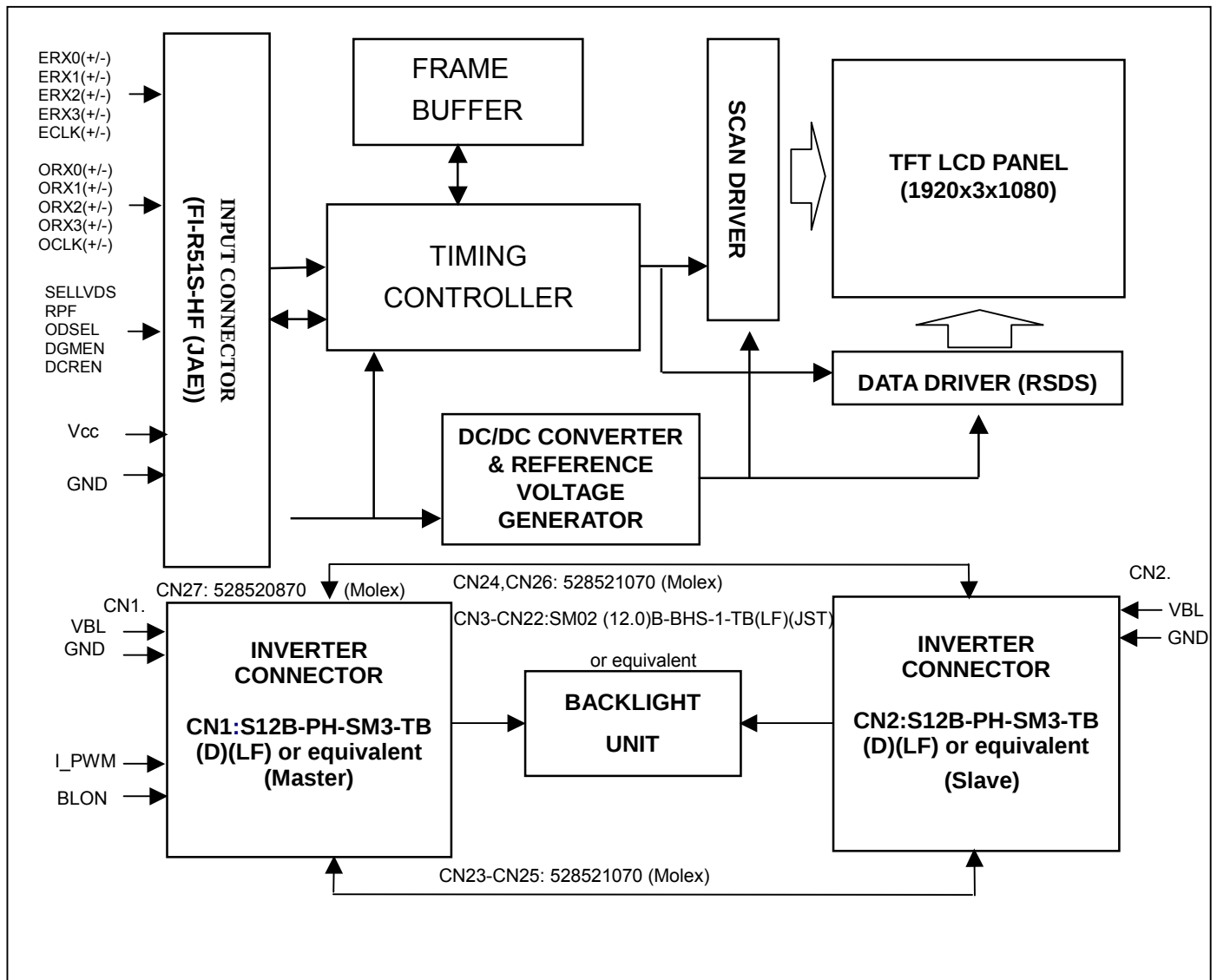
Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	I_PWM	Internal PWM Control Signal
12	BLON	BL ON/OFF

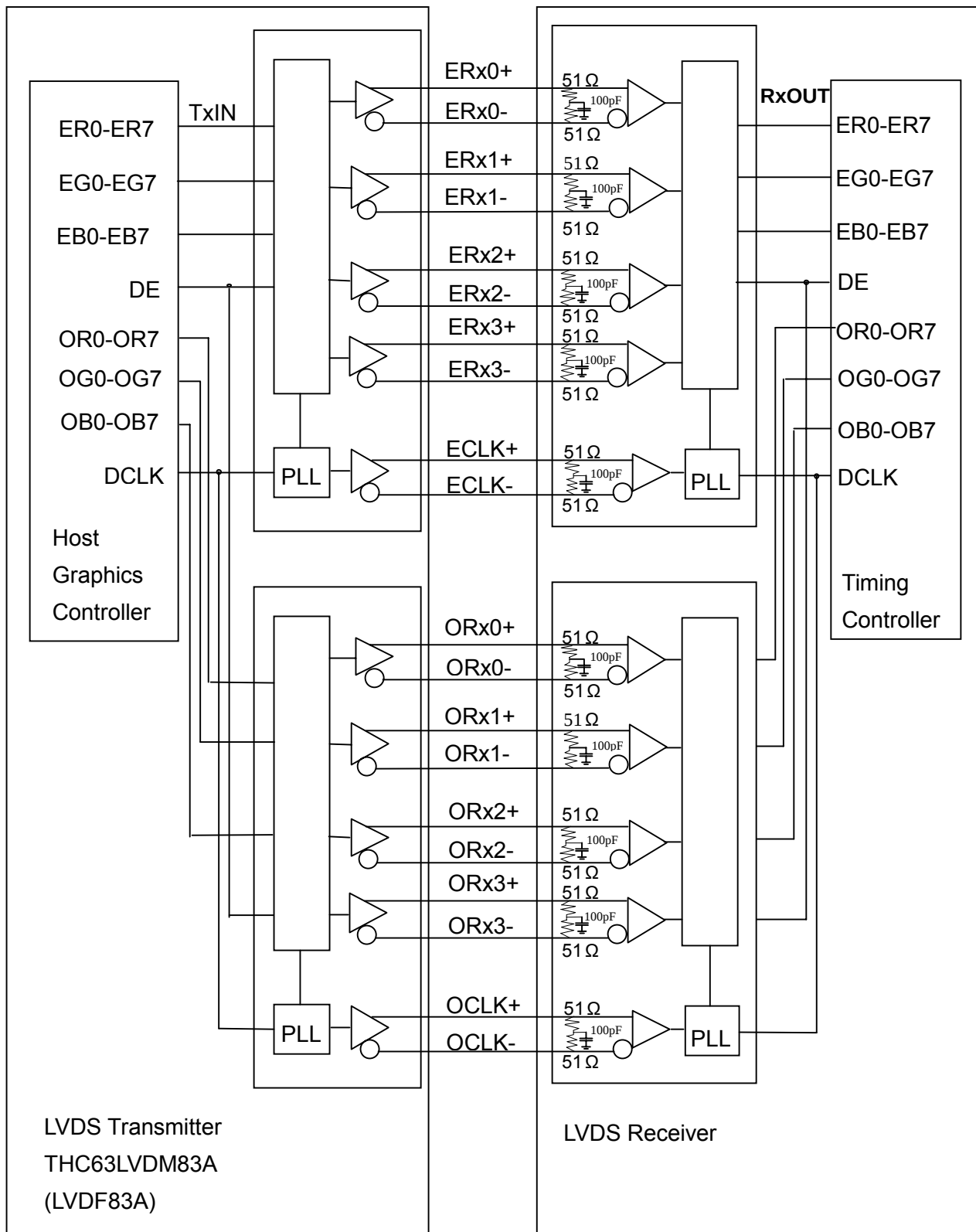
CN2: S12B-PH-SM3-TB(D)(LF)(JST) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC



2.3 BLOCK DIAGRAM OF INTERFACE





ER0~ER7 : Even pixel R data

EG0~EG7 : Even pixel G data

EB0~EB7 : Even pixel B data

OR0~OR7: Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7: Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

- Notes:
- (1) The system must have the transmitter to drive the module.
 - (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
 - (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

2.4 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83 A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	LVDS_SEL =L or OPEN	LVDS_SEL = H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	LVDS_SEL =L or OPEN	LVDS_SEL = H
24 bit	R0	R2	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2			30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
	DCLK		31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK	DCLK	
					TxCLK OUT-	RxCLK IN-		OUT		

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

3. COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1

	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4. INTERFACE TIMING

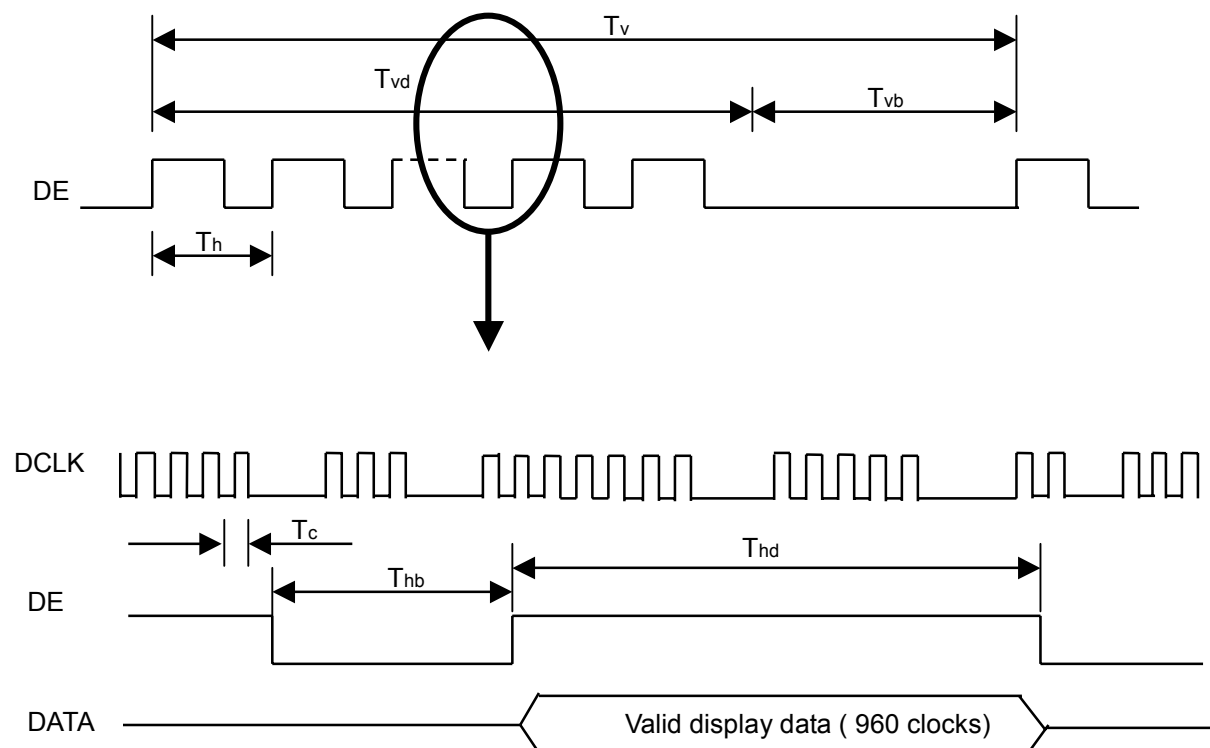
4.1 INPUT SIGNAL TIMING SPECIFICATIONS

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(1)
		Fr6	57	60	63	Hz	(1)
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	2100	2200	2300	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
	Blank	Thb	180	280	380	Tc	-

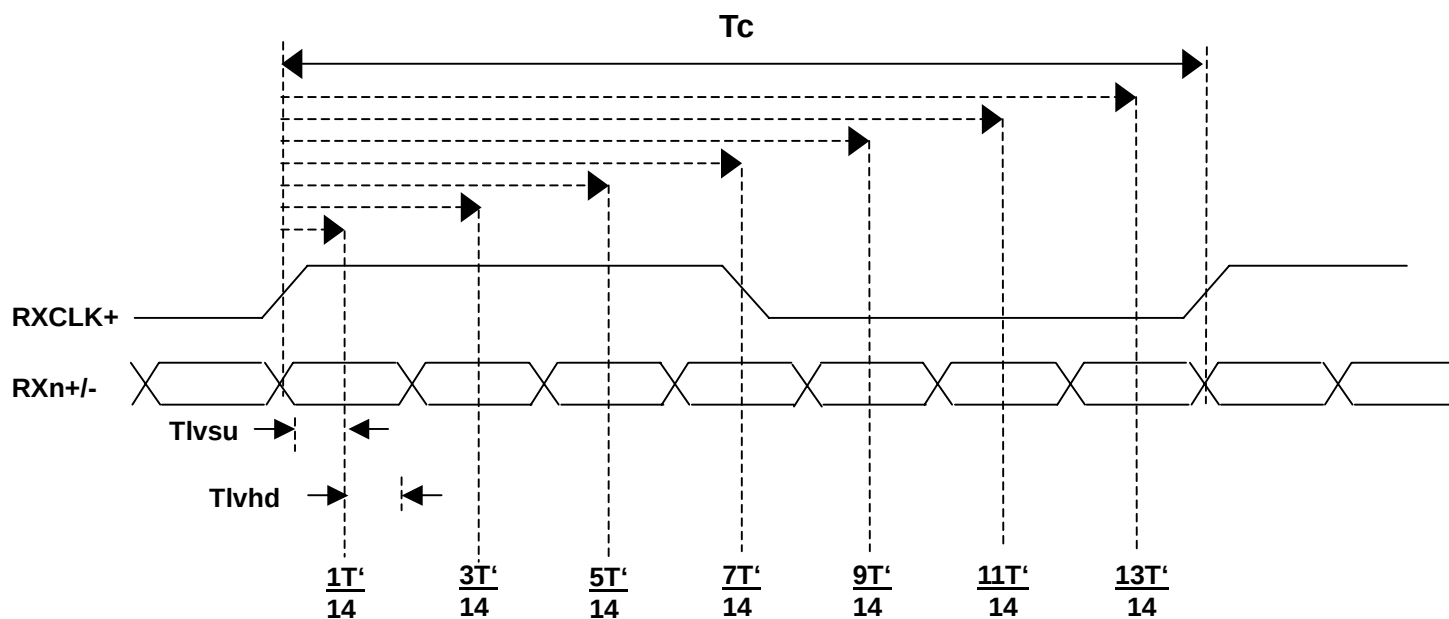
Note (1) (ODSEL) = (H) , (L). Please refer to 5.1 for detail information.

Note (2) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



LVDS INPUT INTERFACE TIMING DIAGRAM



5. PRECAUTIONS

5.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) When storing modules as spares for a long time, the following precaution is necessary.
 - (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 at normal humidity without condensation.
 - (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

5.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.